REMARKS

Applicant thanks Examiner for the detailed review of the application.

Claim Rejections - 35 USC § 112

The Office Action states:

3. Claims 1-13, 25 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 25 have been amended to define the weight of context switch. In regards to claim 1, the weight has been defined as only an instruction pointer, while claim 25 has been amended to having the first weight, which is defined by the user in the independent claim. Furthermore, claim 18 has been clarified to include a context weight less than a full context reduced by general register values, i.e. less than or equal to a full context minus a weight of general register values.

Claim Rejections -35 USC § 102(b)

The Office Action states:

4. **Claims 14-16 and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (hereinafter Wang) (US 2002/0144083 A1).**

"[F]or anticipation under 35 U.S.C. 102, the reference must teach *every aspect* of the claimed invention ..." MPEP 706.02 (emphasis added). "The identical invention must be shown *in as complete detail as contained in the ... claim*." *Richardson v., Suzuki Motor Co*., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

Applicant's claim 14 includes, "a user-modifiable register to specify a user-defined trigger event based on the at least one raw event." Applicant agrees with The Office Action that Wang

discusses switch on event multithreading, as cited by The Office Action in regards to the abstract and paragraphs 0030, 0047, and 0065. However, note that Wang only discusses switching a thread on a trigger, and does not disclose the trigger being specified in a user-modifiable register, as in applicant's claim 14. At paragraph 0047, Wang discloses exemplary triggers, i.e. when a designated instruction is retired or a chaining trigger, but Wang does not discloses that the designated instruction or chaining trigger is specified by a user in a user-modifiable register. In fact, the inference from Wang is that the "designated instruction," is an instruction recognizable as part of an instruction set architecture (ISA) that spawns a thread. In other words, the hardware is designed to recognize the instruction and spawn a thread based on that instruction. In contrast, applicant's claim 14 allows dynamic definition of a specific trigger by a user through modification of a register to specify the trigger event. As described, the trigger event may be a raw event, such as a recognized instruction (dependent claim 16), or a combination of raw events.

The fact that Wang does not contemplate definition of a trigger in a register is found in paragraph 0044, where Wang does disclose common architectural state registers (architecturally visible), i.e. general purpose registers, floating-point registers, predicate registers and control registers (See paragraph 0044), but omits any discussion of these register either being: (1) user-modifiable, or (2) utilized to specify a trigger. Furthermore, paragraph 0065 only discusses examining user-level control or data speculative calculations to determine success or failure. Paragraph 0066 provides an example, where a store conflicts with an earlier load, there is a branch into recovery code. Yet, at no time does Wang disclose user-programmable registers, or that those registers are utilized to define or specify a trigger event.

Claim Rejections -35 USC § 103(a)

The Office Action states:

11. Claims 1-7 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (hereinafter Wang) (US 2002/0144083 A1) in view of Jones et al. (hereinafter Jones) (US 2005/0107986 A1).

"The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). The Office Action has failed to meet one or more of these requirements.

Applicant's claim 1 includes, "thread switch handler logic coupled to the trigger-response mechanism to perform a light-weight thread switch of a first instruction pointer from a first thread with a second instruction pointer of second thread responsive to the user-defined trigger event occurring during execution of the first thread." Applicant respectfully submits that neither Wang or Jones disclose a light weight thread switch of an instruction pointer, and furthermore, neither disclose switching based on a user defined event.

First, Wang only describes switching threads based on a trigger, but does not discuss any thread weight -- the light weight thread having a weight of an instruction pointer, such as in applicant's claim 1. Similarly, Jones does not disclose a weight of a thread switch.

Second, as stated above, Wang only describes thread switching based on a trigger, not a

user-defined trigger. Additionally, Jones describes registers that are user-programmable to monitor performance events, but does not disclose any sort of thread switch trigger, only specific events to be monitored for performance. The only discussion of thread switch is how to handle the values of the performance counters when a switch occurs – they are correspondingly switched as well (see paragraph 0025). However, at no time does Jones disclose that a thread switch is to occur based on the counters/registers or their values, but rather Jones only discloses how to handle the counter values upon a thread switch.

The Office Action further states:

27. Claims 17 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (hereinafter Wang) (US 2002/0144083 A1) in view of Spix et al. (hereinafter Spix) (US 6,195,676).

Applicant's claim 28 includes, "user-programmable event logic coupled to the event detection logic to indicate a user-defined trigger event, the user-defined trigger event to be based on at least the raw event…the thread switch logic, in response to the user-defined trigger event being detected, to save a portion of a first context based on the weight of a context to be saved that is to be specified in the user-programmable context control logic and to spawn a helper thread without operating system intervention." As stated above in reference to claim 14, applicant respectfully submits that Wang only discloses thread switching based on a trigger but does not disclose a trigger being user define or logic that is user-programmable to define a trigger." In fact, the Office Action's combination with regard to claim 1 at page 6 admits that Wang is silent that the thread switching occurs responsive to a user-defined trigger event.

Furthermore, Spix does not disclose user-programmable context control logic to specify a weight of a context. Spix, at col. 3 lines 9-35, does describe a light-weight process – a process that

does not have the full context of a process. In the same paragraph, the only discussion of registers is that a light weight process does not contain a full set of registers for the processor (lines 15-17), which defines the statement that a light weight thread does not contain a full context, and that it may be known at certain points which registers don't have values, which only describes how those register may not be required to be saved as part of a light weight context switch. However, nowhere in the disclosure does Spix describe registers, which are user programmable, that specify the weight of the context. In other words, Spix describes determining the weight at known points based on which registers do not have values, not based on user-programmable registers that define the weight, i.e. how much of the context is to be switched.

The Office Action further states:

33. Claims 21-23 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kissell (US 2005/0050395 A1) in view of Jones et al. (hereinafter Jones) (US 2005/0107986 A1).

Applicant's claim 21 includes, "utilizing hardware to switch an amount of context information of the first thread with the amount of context information of a second thread without operating system intervention, wherein the amount of context information has a first weight that is user-defined in a user-addressable control register." As described above, none of the references disclose an amount of context information that is switched being defined by user in a user-defined control register.

Conclusion

As a result, applicant respectfully submits that independent claims 1, 14, 21, and 2, as well as their dependent claims, are now in condition for allowance for at least the reasons stated above. If there are any additional charges, please charge Deposit Account No. 50-0221. Furthermore, to expedite prosecution of the application, the Examiner is invited to contact David P. McAbee at (503) 712-4988 at any time to schedule a telephone interview in light of potential further rejection of the claims by the Examiner or questions regarding this amendment.

Respectfully submitted,
Intel Corporation

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/David P. McAbee/Reg. No. 58,104
David P. McAbee
Reg. No. 58,104

Intel Corporation
M/S JF3-147
2111 NE 25th Avenue
Hillsboro, OR 97124
Tele – 503-712-4988
Fax – 503-264-1729